What is claimed is:

1. A probe card mountable to a device under test (DUT) board tester for use in a system for testing solder bumps on a wafer, the DUT being connected to a tester, said probe card comprising: a substrate having solder balls on one side and solder on pad (SOP) on the other side; probe pins in contact with the SOP, said probe pins being connected to the substrate via the SOP and being engageable with the solder bumps on the wafer, said probe pins acting as an interface between the tester and the solder bumps.

2. The probe card as recited in claim 1, wherein the substrate is organic.

3. The probe card as recited in claim 1, wherein the substrate is ceramic.

4. The probe card as recited in claim 1, wherein the SOP comprises a first alloy disposed on a second alloy, wherein the second alloy is different than the first alloy.

5. A method of making a probe card mountable to a device under test (DUT) board tester for use in a system for testing solder bumps on a wafer, the DUT being connected to a tester, said method comprising: providing a substrate having solder balls on one side and solder on pad (SOP) on the other side; and attaching probe pins to the SOP, wherein the probe pins are connected to the substrate via the SOP.

6. The method as recited in claim 5, further comprising building up the SOP before attaching the probe pins to the SOP.

7. The method as recited in claim 6, said SOP being formed of a first alloy, wherein the step of building up the SOP before attaching the probe pins to the SOP comprises adding more first alloy to the SOP.

8. The method as recited in claim 6, said SOP being formed of a first alloy, wherein the step of building up the SOP before attaching the probe pins to the SOP comprises adding a second alloy to the first alloy, said second alloy being different than said first alloy.

9. A probe card mountable to a tester for use in a system for measuring package interconnect impedance, the system including the tester, a device under test (DUT)/load board which is configured to retain a substrate, the DUT/load board being connected to the tester, the tester being connected to a Digital Sampling Oscilloscope (DSO) configured to receive a reflected signal from the substrate and provide the reflected signal to the tester, wherein the tester is configured to analyze the reflected signal and provide interconnect impedance versus time data, said probe card comprising: a package having solder balls on a first surface thereof, and a electrically conductive material on a second surface thereof, said electrically conductive surface configured to electrically contact bumps on the substrate.

10. The probe card as recited in claim 9, said solder balls mountable to a test head inter phase board of the tester.

11. The probe card as recited in claim 9, wherein the probe card does not have any probe pins.

12. The probe card as recited in claim 9, wherein the probe card is configured to make electrical contact with bumps on the substrate without using probe pins.

13. A method for measuring package interconnect impedance, said method comprising: providing a tester having a test head; providing a probe card mounted to the test head of the tester, said probe card including a package having solder balls on a first surface thereof mounted to the test head, and an electrically conductive material on a second surface of the package, said electrically conductive surface configured to electrically contact bumps on the substrate, providing a device under test (DUT)/load board which is configured to retain a substrate, said tester being connected to a Digital Sampling Oscilloscope (DSO); contacting said electrically conductive surface of said probe card with bumps on the substrate; using said DSO to launch a signal which is received by the substrate, wherein said DSO is configured to receive a reflected signal from the substrate and provide the reflected signal to the tester; and using post processing software to analyze the reflected signal and provide interconnect impedance versus time data.

14. The method as recited in claim 13, further comprising mounting the probe card to a test head inter phase board of the tester.

15. The method as recited in claim 13, further comprising engaging said probe card with the substrate without using any probe pins.